

The Central Processing Unit (CPU)

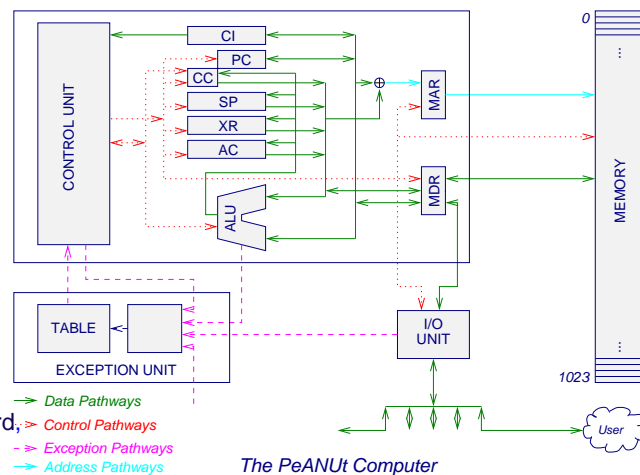
- control unit: responsible for fetching instructions from memory and initial decoding
- arithmetic logic unit (ALU): performs operations such as addition, multiplication, logical AND, logical OR, etc
 - the control unit determines which operation; also the inputs and outputs (registers and/or data)
- registers: small, very fast memory located in the CPU, used to store control information and temporary results
 - program counter (PC): stores address in memory of next instruction to be fetched and executed
 - instruction register (IR): holds current instruction
 - status register (SR): status after operation
 - ◆ e.g. results of last (numeric) comparison, overflow, division-by-zero, etc.
 - other registers (e.g. accumulator, index register, data register, etc)

Executing Machine Instructions

- instructions (of a program) are stored in memory at consecutive addresses
 - usually executed in sequence, with the control unit fetching the instruction using the address from the program counter (PC)
- this repeated process (fetch-decode-execute cycle) is central to CPU operation:
 1. fetch instruction from memory at address PC into instruction register (IR)
 2. update PC to point to the next instruction
 3. determine the type of instruction in the IR (decode)
 4. if it refers to data in memory, determine the address
 5. fetch the data (if any, into the memory data register)
 6. execute the instruction
 7. handle exceptions
 8. store the results into registers (or memory)
 9. go to step 1

CPU Architecture

- e.g. architecture of the PeANUt microprocessor
- the data path indicates the flow of information
- communication events in a typical computer ([O'H&Bryant, figs 1.5-1.7]):
 - read from keyboard,
 - display string,
 - load executable program



The PeANUt Computer

Executing Machine Instructions: Example

registers:

PC:
IR:
MAR:
MDR:
AC:

main memory

address: instruction:
... ..
1A load #3₁₀
1B add 2E
1C store 2E
... ..

2E 4₁₀
result at address 2E₁₆ is 7₁₀

