

Virtual Memory Concerns

- program addresses are virtual; H/W translates these into physical addresses
 - as for caches, this is (largely) transparent to the programmer
- on PeANUt, how many memory references are needed to execute a load instruction? (a) 1 (b) 2 (c) 3 (d) 4
- real machines have (in their MMUs) a translation lookaside buffer (TLB) of T entries
 - effectively a 'cache' of recent VM translations
 - typically $T = 64 \Rightarrow$ a working set of > 64 pages causes TLB misses
 - ◆ usually causes an O.S. trap to access the page tables; costs $10^2 \dots 10^3$ cycles!
 - typically, TLBs are fully associative with an LRU replacement policy
- a working set of T pages is needed to minimize TLB misses
- good locality can also minimize page faults (the swap space is at the very bottom of the memory hierarchy!)
- discussion point: list (at least) 6 similarities between caching and virtual memory