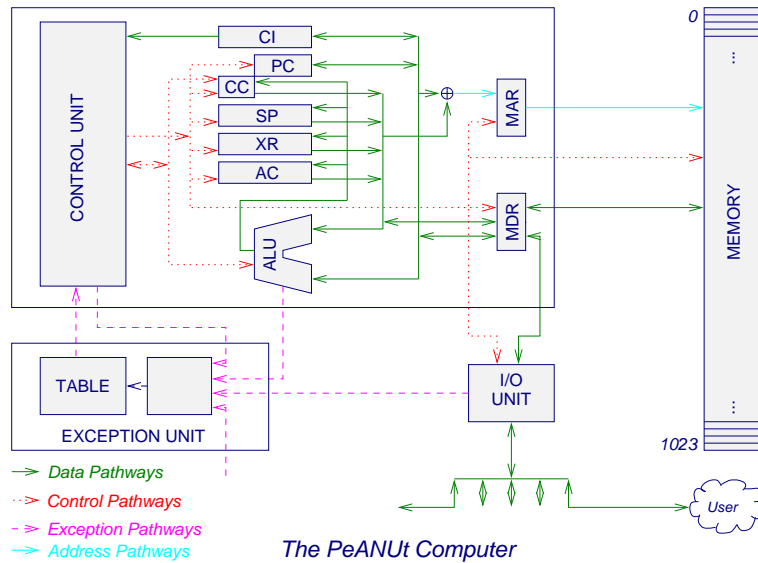


The PeANUt Architecture



Memory Access

- memory contains both programs and data (strings, variables, etc.)
- to read: *(from memory to CPU)*
 1. CPU puts the address in MAR
 2. CPU signals Read, Enable
 3. memory puts the data from the specified address into the MDR
- to write: *(from CPU to memory)*
 1. CPU puts the address in MAR
 2. CPU puts the data in MDR
 3. CPU signals Write, Enable
 4. memory puts MDR contents into the specified address

PeANUt Memory

- 1024 cells (= 1 word)
 - cell addresses 0...1023
 - need 10 address lines ($2^{10} = 1024$)
- each cell has 16 bits (2 bytes)
- there are 3 pathways:
 - address lines (10 bits, input only)
 - data lines (16 bits, input and output)
 - control lines (2 bits, Read/Write, Enable)
- address lines connected to MAR (Memory Address Register) in the CPU
- data lines connected to MDR (Memory Data Register) in the CPU
- control lines connected to the control unit in the CPU

CPU (Central Processing Unit)

- contains:
 - control unit: the circuits that supervise
 - registers (16 bits each)
 - ALU (Arithmetic and Logic Unit)
- PeANUt is a von Neumann architecture ($C = A \text{ op } B$, or $B = A$)

